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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/595,168

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Atsushi Tabuchi

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GLOBAL IP COUNSELORS, LLP
1233 20TH STREET, NW, SUITE 700
WASHINGTON, DC 20036-2680

EXAMINER

SHAH, TUSHAR S

ART UNIT

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/595,168	Applicant(s) TABUCHI, ATSUSHI	
	Examiner TUSHAR S. SHAH	Art Unit 2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 July 2010.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4, 8, 9 and 13-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☐ Claim(s) 1-4, 8, 9, 13-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This action is in response to the amendment filed on July 21st, 2010.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-4, 8, 9, and 13-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stallkamp US Patent No. 6,895,009 B1 (hereinafter Stallkamp) in view of Domon US Publication No. 2003/0014679 A1.

Referring to claim 1, Stallkamp discloses, a data conversion system comprising:

A first and second node in which one of the first and second node (A/V devices 108 and 110, Stallkamp Fig. 1) on an IEEE1394 bus (isochronous network 104 is IEEE 1394 compliant, Stallkamp, column 4, lines 56-60) serves as a cycle master (Master 106, Stallkamp Fig. 1), the second node being having a data conversion unit configured to synchronize second data generated by the conversion of the first data in the second node with an external reference signal, the second not to out put the data,

an external synchronizing signal receiver (SYNC 254, Stallkamp Fig. 2) for receiving an external reference signal (house reference signal 225, Stallkamp Fig. 2) provided on at least one of the first and second nodes (the house reference signal is provided to each node by the bus 102, Stallkamp Figs 1 and 2),

a synchronization adjustment unit for synchronizing a frequency of the cycle start packet output from the cycle master with a frequency of the external reference signal received by the external synchronizing receiver, by carrying out feedback control of a clock source frequency (The synchronizer utilizes a feedback loop 401 to generate a locked cycle time, column 6, lines 30-43) of the cycle master using the external reference signal (Synchronizer 254 synchronizes the operating frequencies of AV devices and enables data based in one time domain to be transmitted over an isochronous bus of a second time domain, Stallkamp column 5, lines 10-20).

It is noted that Stallkamp does not appear to explicitly disclose, the first node being configured to transmit first data to the second node at a transfer rate synchronized with a cycle start packet output from the cycle master.

However, Domon discloses, the first node being configured to transmit first data (Digital Video data is mapped into isochronous packets and received by a digital video player 220, Domon page 6, paragraph 0098 lines 3-8 and paragraph 0099, lines 1-3) to the second node at a transfer rate synchronized with a cycle start packet output from the cycle master (the cycle master outputs a cycle start packet to the other nodes in the network to synchronize them to the master, Domon page 1, paragraph 0017, lines 1-5),

Stallkamp and Domon are analogous art because they are from the same field of endeavor, namely, they both synchronous video data transmitted over an IEEE 1394 bus.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Stallkamp and Domon before him or her, to enhance the communication and conversion methods of Domon with the synchronization with the house reference signal of Stallkamp.

The suggestion/motivation for doing so is present in Stallkamp, column 1 lines 59-67, where it states that A/V data may have been generated based on a clock and rate different from that of the isochronous bus used to transmit it and therefore the house reference signal with allow synchronization with both clock rates.

Therefore it would have been obvious to combine Domon with Stallkamp to obtain the invention as recited in the instant claim.

As per claim 2, it is noted that Stallkamp does not appear to explicitly disclose, the first data and the second data are image data, and the first data is a video signal in DV format and the second data is an analog video signal or SDI video signal.

However Domon discloses, the first data and the second data are image data, and the first data is a video signal in DV format and the second data is an analog video signal or SDI video signal (the digital video player 220 decodes the DV format data and outputs an analog video signal, Domon page 6, paragraph 0098, lines 6-8).

Stallkamp and Domon are analogous art because they are from the same field of endeavor, namely, they both synchronous video data transmitted over an IEEE 1394 bus.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Stallkamp and Domon before him or her, to enhance the communication and conversion methods of Domon with the synchronization with the house reference signal of Stallkamp.

The suggestion/motivation for doing so is present in Stallkamp, column 1 lines 59-67, where it states that A/V data may have been generated based on a clock and rate different from that of the isochronous bus used to transmit it and therefore the house reference signal with allow synchronization with both clock rates.

Therefore it would have been obvious to combine Domon with Stallkamp to obtain the invention as recited in the instant claim.

As per claim 3, the first node serves as cycle master for data transfer (AV devices 108 and 110 may function as the cycle master and maybe a device such as a digital video camera, Stallkamp column 3, lines 17-19 and 37-41).

As per claim 4, Stallkamp discloses, the second node comprises a second synchronization adjustment unit (SYNC 254, Stallkamp Fig. 2),

the frequency of the cycle start packet is linked with the frequency of the reference signal (Synchronizer 254 synchronizes the operating frequencies of AV

devices and enables data based in one time domain to be transmitted over an isochronous bus of a second time domain, Stallkamp column 5, lines 10-20) by the synchronization adjustment unit of the node that serves as the cycle master (Either AV node 108 or AV node 110 may serve as cycle master, column 3, lines 37-41) (Therefore the second node, node, whether 108 or 110, may serve as the cycle master and synchronize itself internally).

Referring to claim 8, similar limitations as in claim 1 are recited. Therefore the rejection of claim 1 applies to claim 8.

As per claim 9, similar limitations as in claim 2 are recited. Therefore the rejection of claim 2 applies to claim 9.

As per claim 13, it is noted that Stallkamp does not appear to explicitly disclose, the first node is hardware comprising an 13940HCI compliant IEEE1394 interface for outputting a video signal in DV format as first data, and the second node is data conversion hardware for outputting an analog video signal or SDI video signal as second data.

However, Domon discloses, the first node is hardware comprising an 13940HCI compliant IEEE1394 interface for outputting a video signal in DV format as first data, and the second node is data conversion hardware for outputting an analog video signal or SDI video signal as second data (the digital video player 220 decodes a digital video

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signal of DV format received from the IEEE1394 bus and outputs an analog video signal, Domon page 6, paragraph 0098, lines 6-8)..

Stallkamp and Domon are analogous art because they are from the same field of endeavor, namely, they both synchronous video data transmitted over an IEEE 1394 bus.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Stallkamp and Domon before him or her, to enhance the communication and conversion methods of Domon with the synchronization with the house reference signal of Stallkamp.

The suggestion/motivation for doing so is present in Stallkamp, column 1 lines 59-67, where it states that A/V data may have been generated based on a clock and rate different from that of the isochronous bus used to transmit it and therefore the house reference signal with allow synchronization with both clock rates.

Therefore it would have been obvious to combine Domon with Stallkamp to obtain the invention as recited in the instant claim.

As per claim 14, Stallkamp discloses, the second node comprises the external synchronizing signal receiver and synchronization adjustment unit (both nodes receive the house reference clock 102, and contain a Sync unit 254, Fig. 2), and serves as cycle master for data transfer (column 3, lines 36-42).

As per claim 15, Stallkamp discloses, the first node comprises the synchronization adjustment unit, the second node comprises the external synchronizing signal receiver and synchronization adjustment unit (both nodes receive the house reference clock 102, and contain a Sync unit 254, Fig. 2),

It is noted that Stallkamp does not appear to explicitly disclose, the cycle start packet frequency is synchronized with the frequency of the external reference signal received by the external synchronizing signal receiver by means of the synchronization adjustment unit of the node that serves as cycle master.

However, Domon discloses, the cycle start packet frequency is synchronized with the frequency of the external reference signal received by the external synchronizing signal receiver by means of the synchronization adjustment unit of the node that serves as cycle master (the cycle master outputs a cycle start packet to the other nodes in the network to synchronize them to the master, Domon page 1, paragraph 0017, lines 1-5),

Stallkamp and Domon are analogous art because they are from the same field of endeavor, namely, they both synchronous video data transmitted over an IEEE 1394 bus.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Stallkamp and Domon before him or her, to enhance the communication and conversion methods of Domon with the synchronization with the house reference signal of Stallkamp.

The suggestion/motivation for doing so is present in Stallkamp, column 1 lines 59-67, where it states that A/V data may have been generated based on a clock and

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rate different from that of the isochronous bus used to transmit it and therefore the house reference signal with allow synchronization with both clock rates.

Therefore it would have been obvious to combine Domon with Stallkamp to obtain the invention as recited in the instant claim.

As per claim 16, Stallkamp discloses, when the first node serves as cycle master, the external reference signal received by the external synchronizing signal receiver of the second node is transmitted from the second node to the first node by asynchronous transfer of an IEEE 1394 interface (column 3, lines 50-54).

As per claim 17, Stallkamp discloses, a dedicated synchronization signal line for transmitting the external reference signal received by the external synchronizing signal receiver of the second node from the second node to the first node when the first node serves as cycle master (House reference clock 102, Figs 1 and 2).

As per claim 18, Stallkamp discloses, the first node comprises the external synchronizing signal receiver and synchronization adjustment unit (both nodes receive the house reference clock 102, and contain a Sync unit 254, Fig. 2), and serves as cycle master for data transfer (column 3, lines 36-42).

As per claim 19, Stallkamp discloses, one of the first node and the second node serves and the cycle master (column 3, lines 36-42) and the other of the first node and

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the second node includes the synchronization adjustment unit (both nodes receive the house reference clock 102, and contain a Sync unit 254, Fig. 2).

Response to Arguments

3. Applicant's arguments filed 7/21/2010 have been fully considered but they are not persuasive.

Regarding independent claim 1, the applicant argues, on pages 7-8 of the response, that neither Stallkamp nor Domon appear to explicitly disclose, a synchronization adjustment unit for synchronizing a frequency of the cycle start packet output from the cycle master with a frequency of the external reference signal received by the external synchronizing receiver, by carrying out feedback control of a clock source frequency of the cycle master using the external reference signal.

The examiner disagrees. the Sync unit 254 of Stallkamp, provided on each node, receives the reference signal 102 and the isochronous signal of the IEEE1394 bus, and utilizes a feedback loop based logic block to generate the video clock 310. See Figs. 2-4, column 6, lines 1-23.

Finally regarding independent claim 1, the applicant has argued, on page 9 of the response, that the combination of Stallkamp and Domon would not be obvious.

The examiner disagrees. The motivation for combining the conversion methods of Domon with the synchronization methods of Stallkamp is explicitly taught in Stallkamp. See column 1, lines 59-67 and lines 1-12. Specifically stated here is the need to synchronize the isochronous network, which is based upon the cycle start packet, with the reference signal, in order to prevent the clocks from drifting apart and adversely affecting video playback. The Domon reference discusses transmitting video data between nodes over a 1394 bus but does not provide for synchronization, and therefore the Stallkamp reference remedies this deficiency.

The grounds of rejection to claim 1 are maintained.

Regarding the remaining claims 2-4, 8, 9 and 13-19, the applicant has argued that these claims are allowable for the same reasons as claim 1. As the issues with claim 1 are seen as being overcome, the grounds of rejection to these claims are also maintained.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

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shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TUSHAR S. SHAH whose telephone number is (571)270-1970. The examiner can normally be reached on Mon-Fri 7:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Henry Tsai can be reached on 571-272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/T. S. S./

/Henry W.H. Tsai/
Supervisory Patent Examiner, Art Unit 2184